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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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575 Madison Ave.  
New York, NY 10022-2585

EXAMINER

BELLO, AGUSTIN

ART UNIT	PAPER NUMBER
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2633

DATE MAILED: 04/11/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

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## Office Action Summary

Application No.

09/478,604

Applicant(s)

IDE ET AL.

Examiner

Agustin Bello

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 January 2003.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-39 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All   b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                             | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 4, 7-11, 13, 16-19, 22, 25-28, 34, and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (U.S. Patent No. 5,475,342) in view of Crimmins (U.S. Patent No. 5,319,191).

Regarding Claims 1, 4, 10, 13, 19, 22, 28, and 34, Nakamura teaches a burst signal detection circuit comprising: a DC variation removing circuit (reference numeral BC1 in Figure 6) for detecting the bottom level or the peak level of an input signal and removing the DC level variation of the input signal based on the bottom level or the peak level; and an amplitude identifying circuit (reference numeral BC2 in Figure 6) for detecting the presence or absence of a burst signal in said input signal based on the output signal from the DC variation removing circuit; said amplitude identifying circuit including: an amplitude detection circuit (reference numeral 20 in Figure 6) for detecting the maximum amplitude of the output signal of said DC variation removing circuit; a threshold level control circuit for controlling a threshold level (reference numeral 10 in Figure 6); and a comparator circuit (reference numeral 40 in Figure 6) for comparing and outputting a detection signal indicating the presence or absence of the burst signal. Nakamura differs from the claimed invention in that Nakamura fails to specifically teach that the comparator compares the output level of said amplitude detection circuit with said

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threshold level. However, Crimmins, in the same field of endeavor, teaches it is well known in the art to compare the output level of an amplitude detection circuit with a threshold level generated by a threshold control circuit (reference numerals 58, 62, 69, 73, 64, 96, 100, 101, 104, 108 in Figure 1). One skilled in the art would clearly have recognized that one could have determined whether or not a burst signal was present via the method taught by Crimmins. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have compared the output level of said amplitude detection circuit with the threshold level generated by the threshold control circuit, as taught by Crimmins, in order to determine the presence of a burst signal.

Regarding Claims 2 and 11, Nakamura teaches the burst signal detection circuit according to claim 1, wherein said DC variation removing circuit includes a bottom detection circuit or a peak detection circuit for detecting the bottom level or the peak level, respectively, of the input signal (reference numeral 10 in BC1 of Figure 6), and a differential amplifier (reference numeral 40 in BC1 of Figure 6) for differentially amplifying the difference between the input signal and the output signal from said bottom detection circuit or said peak detection circuit.

Regarding Claims 7, 16, 25, and 37 the combination of references differs from the claimed invention in that it fails to specifically teach that said threshold level control circuit includes a temperature compensating circuit for changing said threshold level in accordance with the temperature change, said temperature compensating circuit being so configured as to compensate for the variation of the gain due to the temperature change. However, temperature compensation circuits in the form of resistors and thermistors are very well known in the art and are used by those skilled in the art as a means for temperature compensation. Furthermore, it is

well known in the art that there is a direct correlation between the temperature change of a gain circuit and the gain performance of that circuit. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have included a temperature compensation circuit in order to compensate for the variation of the gain due to the temperature change.

Regarding Claims 8, 17, 26, and 38, the combination of references differs from the claimed invention in that it fails to specifically teach that said threshold level control circuit includes a reference voltage circuit for changing said threshold level with the source voltage change, said reference voltage circuit being so configured as to compensate for the variation of the gain due to the supply voltage change. However reference voltage circuits in the form of source voltage are very well known in the art and are used by those skilled in the art as a means for changing the threshold level of a circuit. Furthermore, it is well known in the art that there is a direct correlation between input voltage of a gain circuit and the gain performance of that circuit. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have included a reference voltage circuit in order to compensate for the variation of the gain due to the supply voltage change.

Regarding Claims, 9, 18, 27, and 39, Nakamura teaches a photo-diode (reference numeral 1 in Figure 2) for receiving an optical signal and a preamplifier (reference numeral 2 in Figure 2) for converting the current signal from said photo-diode into a voltage signal, wherein the arrival of a burst signal is detected from the output signal of said preamplifier (see Figure 6).

3. Claims 3, 5, 6, 12, 14, 15, 23, 24, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Crimmins and Shimizu (U.S. Patent No. 6,38,049).

Regarding Claims 3, 5, 12, 14, 23, and 35, the combination of Nakamura and Crimmins teaches the burst signal detection circuit according to claim 1, wherein said DC variation removing circuit includes: a bottom detection circuit or a peak detection circuit for detecting the bottom level or the peak level, respectively, of the input signal, and a differential amplifier (as seen in Figure 6). The combination of Nakamura and Crimmins differs from the claimed invention in that it fails to specifically teach a level shift circuit for shifting the output signal of said bottom detection circuit or said peak detection circuit by a predetermined value, wherein the differential amplifier amplifies the difference between the output signal of said level shift circuit and the input signal. However, the use of level shift circuits is well known in the art. For example, Shimizu, in the same field of endeavor, teaches it is well known in the art to use a level shift circuit (reference numeral 62 in Figure 1) for shifting the output signal of said bottom detection circuit or said peak detection circuit by a predetermined value. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have used a level shift circuit as taught by Shimizu in the device of the combination of Nakamura and Crimmins for shifting the output signal of said bottom detection circuit or said peak detection circuit by a predetermined value.

Regarding Claims 6, 15, 24, and 36, the combination of Nakamura and Crimmins differs from the claimed invention in that it fails to specifically teach a threshold level control circuit for generating a first threshold level by shifting the output level of said bottom detection circuit by a predetermined value and generating a second threshold level by shifting the output level of said peak detection circuit by a predetermined value; and a comparator circuit for comparing said first threshold level and said second threshold level with each other. However, as discussed above,

the use of level shift circuits are well known in the art and would have been obvious to one skilled in the art. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have created a second threshold level via a level shift circuit for shifting the level of the peak detection circuit in the device of the combination of Nakamura and Crimmins in accordance with the teachings of Shimizu.

4. Claims 20, 21, and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Crimmins and Nobuhara (U.S. Patent No. 6,115,163).

Regarding Claim 20, the combination of Nakamura and Crimmins teaches said amplitude detection circuit includes a master bottom detection circuit or a master peak detection circuit for detecting the absolute minimum level or the absolute maximum level, respectively, of said input signal, respectively, and a slave peak detection circuit or a slave bottom detection circuit for detecting the relative maximum level or the relative minimum level, respectively, of said input signal, but differs from the claimed invention in that it fails to specifically teach that the slave detecting circuit receives a signal from the output level of said master bottom detection circuit or said master peak detection circuit. However, such a configuration is well known in the art. Nobuhara, in the same field of endeavor, teaches it is well known in the art to have a slave and master detection circuit connected so that the output of the master detection circuit is input to the slave detection circuit (reference numeral 14 in Figure 11). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have configured the amplitude detection circuit of the combination of Nakamura and Crimmins so that the output of the master detection circuit is input to the slave detection circuit as taught by Nobuhara.

Regarding Claim 21, the combination of references and Nobuhara in particular teaches that a level hold capacitor in said slave peak detection circuit or said slave bottom detection circuit of said master-slave type amplitude detection circuit is connected to the output of said master bottom detection circuit or said master peak detection circuit (reference numeral 14 in Figure 11 of Nobuhara).

Regarding Claims 30 and 31, the combination of Nakamura, Crimmins, and Nobuhara teaches that said DC variation removing signal amplifier includes a master-slave type automatic threshold control circuit having: a master bottom detection circuit or a master peak detection circuit for detecting the absolute minimum level or the absolute maximum level, respectively, of said input signal; a slave peak detection circuit or a slave bottom detection circuit for detecting the relative maximum level or the relative minimum level, respectively, of said input signal from the output signal of said master bottom detection circuit or said master peak detection circuit (as discussed above); and a voltage dividing circuit (reference numeral R1, R2 in Figure 4 of Nakamura) for generating a threshold level by dividing the output signal of said master bottom detection circuit or said master peak detection circuit and the output signal of said slave peak detection circuit or said slave bottom detection circuit.

Regarding Claims 32 and 33, the combination of references and Nobuhara in particular teaches the burst signal detection circuit according to claim 30, wherein the level hold capacitor of said slave peak detection circuit or said slave bottom detection circuit of said master-slave automatic threshold control circuit is connected to the output of said master bottom detection circuit or said master peak detection circuit (see Figure 11 of Nobuhara).



5. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Crimmins and Hatakeyama (U.S. Patent No. 6,018,407).

Regarding Claim 29, the combination of Nakamura and Crimmins teaches said DC variation removing signal amplifier which includes: a bottom detection circuit or a peak detection circuit for detecting the DC level variation of said input signal; and an amplifier supplied with said input signal and the output signal of said bottom detection circuit or said peak detection circuit (see BC1 of Figure 6 of Nakamura); However, the combination of Nakamura and Crimmins differs from the claimed invention in that it fails to specifically teach that the negative phase output of said amplifier being fed back to the positive phase input side of said amplifier through a feedback resistor; and the positive phase output of said amplifier being fed back to the negative phase input side of said amplifier through said peak detection circuit and a feedback resistor. However, such this circuit configuration is well known in the art. For example, Hatakeyama, teaches it is well known in the art to connect the negative phase output of an amplifier to the positive phase input side of said amplifier and the positive phase output of said amplifier fed back to the negative phase input side of said amplifier through a peak detection circuit (see Figure 6). Furthermore, the use of feedback resistors is very well known in the art. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have connected the DC variation removing circuit so that the negative phase output of said amplifier being fed back to the positive phase input side of said amplifier through a feedback resistor; and the positive phase output of said amplifier being fed back to the negative phase input side of said amplifier through said peak detection circuit and a feedback resistor, as taught by Hatakeyama.

***Response to Arguments***

6. Applicant's arguments filed 1/30/03 have been fully considered but they are not persuasive. The applicant argues that the Nakamura reference fails to specifically teach or suggest the applicant's DC variation removing circuit for removing the DC component of the input signal by differentially amplifying the difference between the input signal level and one of the peak level and bottom level of the input signal. However, Nakamura clearly discloses a differential amplifier that amplifies the difference between the input signal and one of the peak level and bottom level of the input signal. Nakamura teaches that the limiting amplifier 40 of Figure 6 relied upon by the examiner to teach the limitations claimed, is comprised of a differential amplifier (column 16 line 10 – column 17 line 45 and reference numeral 101A of Figure 15). As such it is clear the Nakamura teaches the applicant's DC variation removing circuit for removing the DC component of the input signal by differentially amplifying the difference between the input signal level and one of the peak level and bottom level of the input signal.

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ota, Ikeda, and Asano teach similar circuits.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (703)308-1393. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (703)305-4729. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

AB

April 4, 2003

  
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